In the Claims:

Please cancel claims 3, 9, 15, and 20 without prejudice.

Please amend claims 1, 17, and 18 as follows:

1. (currently amended)   A method for detecting degradation in an integrated circuit comprising the steps of:

providing a monitor built-in self-test (MBIST) engine;

providing MBIST control circuitry and MBIST registers with said MBIST engine;

providing at least one monitor element coupled to said MBIST engine; said at least one monitor element being defined by predefined circuit elements in the integrated circuit;

providing latch circuitry coupled to said MBIST engine, said latch circuitry used to communicate monitor bits with said MBIST engine;

utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits; and

identifying degradation of signal, timing and voltage margins utilizing said at least one monitor element; and

using said at least one monitor element with said MBIST engine to identify an approaching failing situation for enabling appropriate preventative action.

2. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element defined

by unused circuit elements or instantiations of said unused circuit elements in the integrated circuit.

3. (canceled)

4. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element used as a monitor bit line.

5. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element used as a monitor word line.

6. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element defined by a separate monitor array; said separate monitor array including unique word lines, bit lines, and control and sense circuitry.

7. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said separate monitor array is placed proximate to said MBIST engine.

8. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 the step of providing at least one monitor element coupled to said MBIST engine includes the steps of providing at least one monitor element applied to at

least one of data arrays and registers; said at least one monitor element used with said MBIST engine to insure correct operation of said at least one of data arrays and registers with a defined degree of margin.

9. (canceled)

10. (original)	A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of generating a predefined data pattern utilizing said MBIST engine.

11. (original)	A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by at least one monitor bit line of a memory array; and the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of writing monitor bits with refresh commands.

12. (original)	A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by at least one monitor bit line of a memory array; and the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of writing monitor bits by accessing each row location with said MBIST engine generating a predefined data pattern.

13. (original)	A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by at least one monitor word line of a memory array; and the step of utilizing said MBIST engine

for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of writing monitor bits with refresh commands with said MBIST engine generating a predefined data pattern.

14. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 wherein the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of providing MBIST control circuitry for initializing monitor bits to a known value; utilizing said MBIST control circuitry to control one or more functions including access, restore, address control, data generation, data compare, and refresh functions associated with the monitor bits.

15. (canceled)

16. (original)   A method for detecting degradation in an integrated circuit as recited in claim 1 wherein said at least one monitor element is defined by a separate array and the step of utilizing said MBIST engine for controlling operation of said at least one monitor element and communicating monitor bits includes the steps of generating one of a fixed predefined data pattern or a dynamically changing data pattern utilizing said MBIST engine.

17. (currently amended)   Apparatus for detecting degradation in an integrated circuit and the integrated circuit includes a memory array, said apparatus comprising:

a monitor built-in self-test (MBIST) engine;

said MBIST engine including MBIST control circuitry and MBIST registers;

at least one monitor element coupled to said MBIST engine; said at least one monitor element including at least one of a monitor bit line of the memory array, a monitor word line of the memory array or a separate array including unique word lines, bit lines, and control and sense circuitry;

said MBIST engine for controlling operation of said at least one monitor element for communicating monitor bits; and for identifying degradation of signal, timing and voltage margins utilizing said at least one monitor element;

said at least one monitor element applied to at least one of data arrays and registers; said at least one monitor element used with said MBIST engine to insure correct operation of said at least one of data arrays and registers with a defined degree of margin;

said at least one monitor element being used with said MBIST engine to identify an approaching failing situation for enabling appropriate preventative action; and

latch circuitry coupled to said MBIST engine for latching monitor bits, said latch circuitry used to communicate with said MBIST engine.

18. (currently amended) Apparatus for detecting degradation in an integrated circuit as recited in claim 17 wherein said MBIST engine includes MBIST control circuitry and MBIST registers coupled by said latch circuitry to said at least one monitor element.

19. (original) Apparatus for detecting degradation in an integrated circuit as recited in claim 17 wherein at least one monitor element includes unused circuit elements or instantiations of said unused circuit elements in the integrated circuit.

20. (canceled)